ispLSI® and pLSI® 3256

High Density Programmable Logic

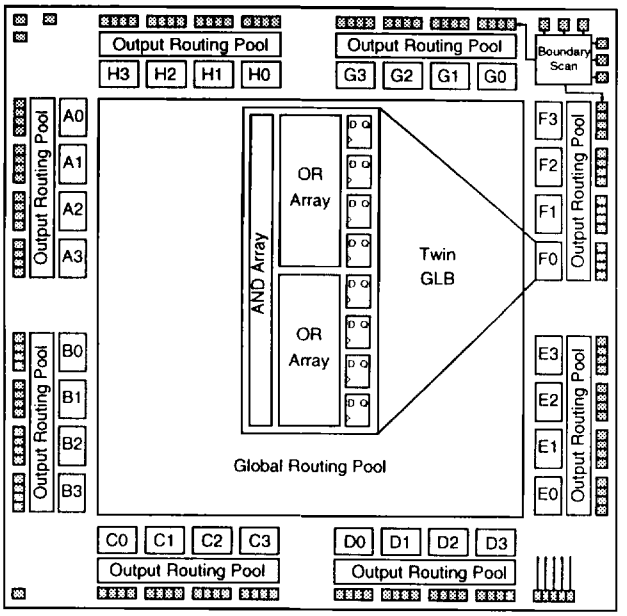
Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - — High Speed Global Interconnect
  - — 128 I/O Pins
  - — 11000 PLD Gates
  - — 384 Registers
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 77 MHz Maximum Operating Frequency
  - — t_{pd} = 15 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - — In-System Programmable 5-Volt Only
  - — Change Logic and Interconnects "On-the-Fly" in Seconds
  - — Reprogram Soldered Devices for Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - — Five Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control to Minimize Switching Noise
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
- **pLSI/ispLSI DEVELOPMENT SYSTEM (pDS®)**

  pDS Software
  - — Easy to Use PC Windows™ Interface
  - — Boolean Logic Compiler
  - — Manual Partitioning
  - — Automatic Place and Route
  - — Static Timing Table

  pDS+™ Software
  - — Industry Standard, Third Party Design Environments
  - — Schematic Capture, State Machine, HDL
  - — Automatic Partitioning and Place and Route
  - — Comprehensive Logic and Timing Simulation
  - — PC and Workstation Platforms

Functional Block Diagram



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Description

The Lattice ispLSI and pLSI 3256 are High Density Programmable Logic Devices which contain 384 Registers, 128 Universal I/O pins, five Dedicated Clock Input Pins, eight Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3256 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3256 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3256 devices, but multiplexes four input pins to control in-system programming.

The basic unit of logic on the ispLSI and pLSI 3256 devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...H3. There are a total of 32 of these Twin GLBs in the ispLSI and pLSI 3256 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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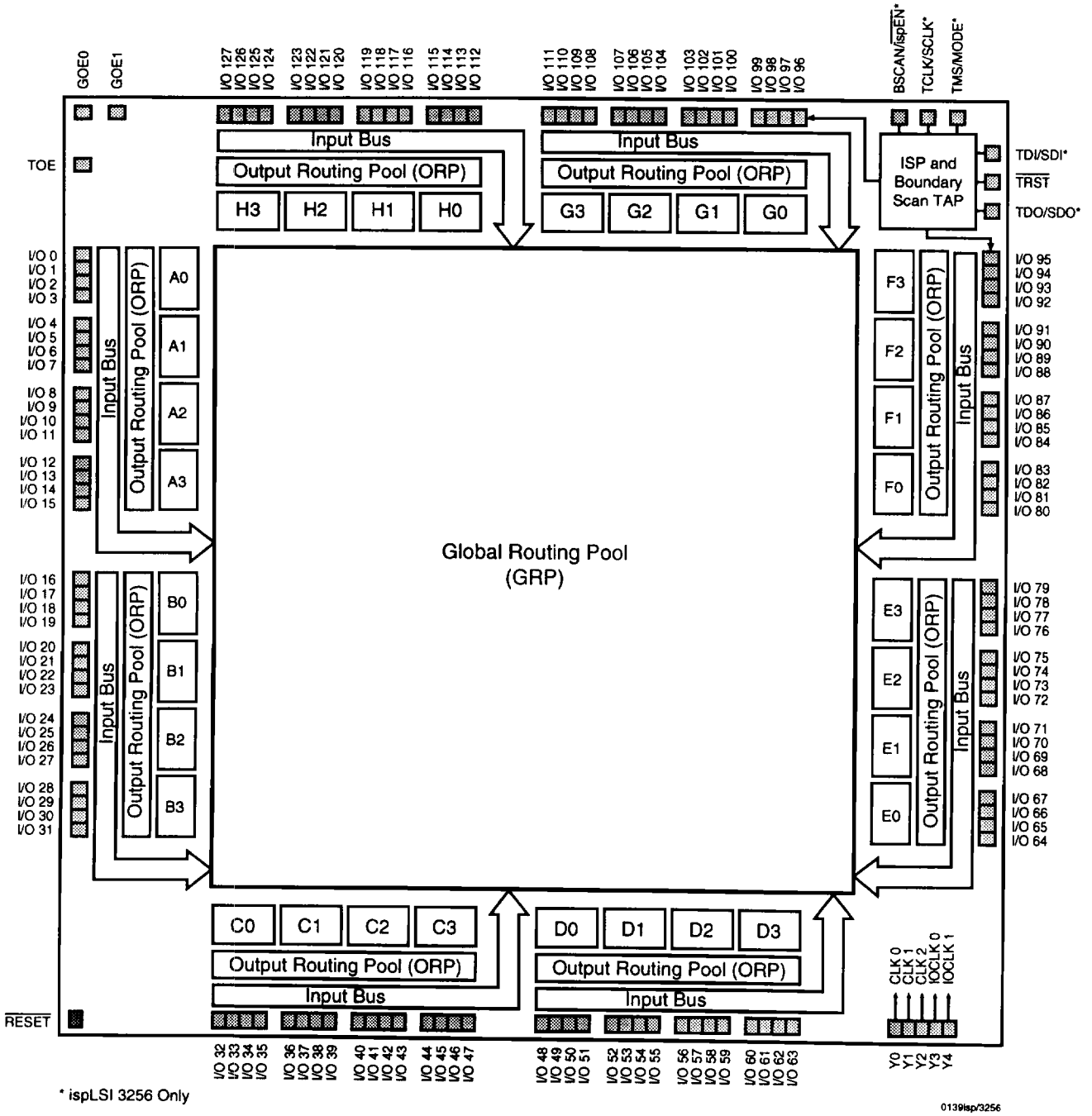
Order #: DS0059

Functional Block Diagram

Figure 1. ispLSI and pLSI 3256 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 128 I/O Cells are grouped into eight sets of 16 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. These groups of 16 I/O cells share one Product Term Output Enable and two Global Output Enable signals.

Four Twin GLBs, 16 I/O Cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI and pLSI 3256 Device contains eight of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3256 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3256 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3256 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI and pLSI 3256

DEVICE	ispLSI and pLSI 3256
Twin GLBs	32
Registers	384
I/O Pins	128
Global Clocks	5
Global OE	2
Test OE	1

Table 1 - 0003Aisp/3256

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Ambient Temp. with Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2 - 0005/3256

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC}= 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	12	pf	V_{CC}= 5.0V, V_Y = 2.0V

1. Guaranteed but not 100% tested.

Table 2 - 0006/3256

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	1000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2 - 0008A-2032-isp

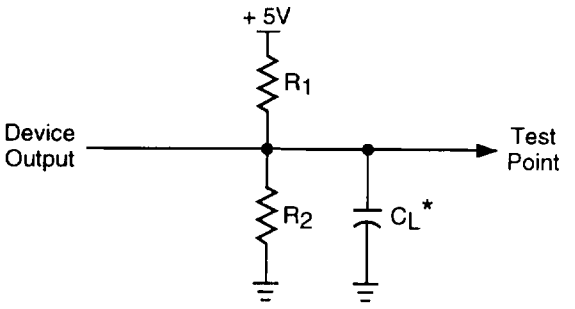
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load conditions (See figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} -0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	Bscan/ispEN Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	-45	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	–	150	270	mA

Table 2 - 0007isp/3256

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using sixteen 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-70		-50		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	15.0	–	20.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	18.0	–	24.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	77	–	57	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	50	–	37	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle[4]	83	–	63	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	9.5	–	12.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	9.0	–	12.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	11.0	–	15.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	10.5	–	14.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	15.0	–	20.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	10.0	–	13.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	18.0	–	24.5	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	18.0	–	24.5	ns
t_{goeen}	B	16	Global OE Output Enable	–	11.0	–	13.5	ns
t_{goedis}	C	17	Global OE Output Disable	–	11.0	–	13.5	ns
t_{toeen}	B	18	Test OE Output Enable	–	17.0	–	23.0	ns
t_{toedis}	C	19	Test OE Output Disable	–	17.0	–	23.0	ns
t_{wh}	–	20	External Synchronous Clock Pulse Duration, High	6.0	–	8.0	–	ns
t_{wl}	–	21	External Synchronous Clock Pulse Duration, Low	6.0	–	8.0	–	ns
t_{su3}	–	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	5.0	–	7.0	–	ns
t_{h3}	–	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0.0	–	0.0	–	ns

Table 2 - 0030A/3256

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions Section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	2.4	–	3.3	ns
t_{iolat}	25	I/O Latch Delay	–	2.4	–	3.3	ns
t_{iosu}	26	I/O Register Setup Time before Clock	6.2	–	8.6	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	3.9	–	5.3	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	1.9	–	2.6	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	3.6	–	4.9	ns
GRP							
t_{grp}	30	GRP Delay	–	3.0	–	4.1	ns
GLB							
t_{4ptbp}	31	4 Product Term Bypass Path Delay	–	5.9	–	7.6	ns
t_{1ptxor}	32	1 Product Term/XOR Path Delay	–	6.4	–	8.8	ns
$t_{20ptxor}$	33	20 Product Term/XOR Path Delay	–	7.4	–	10.1	ns
t_{xoradj}	34	XOR Adjacent Path Delay[3]	–	8.1	–	11.1	ns
t_{gbp}	35	GLB Register Bypass Delay	–	0.1	–	0.1	ns
t_{gsu}	36	GLB Register Setup Time before Clock	1.8	–	2.4	–	ns
t_{gh}	37	GLB Register Hold Time after Clock	6.0	–	8.2	–	ns
t_{gco}	38	GLB Register Clock to Output Delay	–	1.8	–	2.2	ns
t_{gro}	39	GLB Register Reset to Output Delay	–	2.8	–	3.8	ns
t_{ptre}	40	GLB Product Term Reset to Register Delay	–	10.5	–	14.2	ns
t_{ptoe}	41	GLB Product Term Output Enable to I/O Cell Delay	–	5.4	–	7.3	ns
t_{ptck}	42	GLB Product Term Clock Delay	3.2	6.3	4.3	8.5	ns
ORP							
t_{orp}	43	ORP Delay	–	2.7	–	3.6	ns
t_{orpbp}	44	ORP Bypass Delay	–	1.2	–	1.6	ns

Table 2 - 0036A/3256

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR Adjacent path can only be used by Lattice Hard Macros.

Internal Timing Parameters[1]

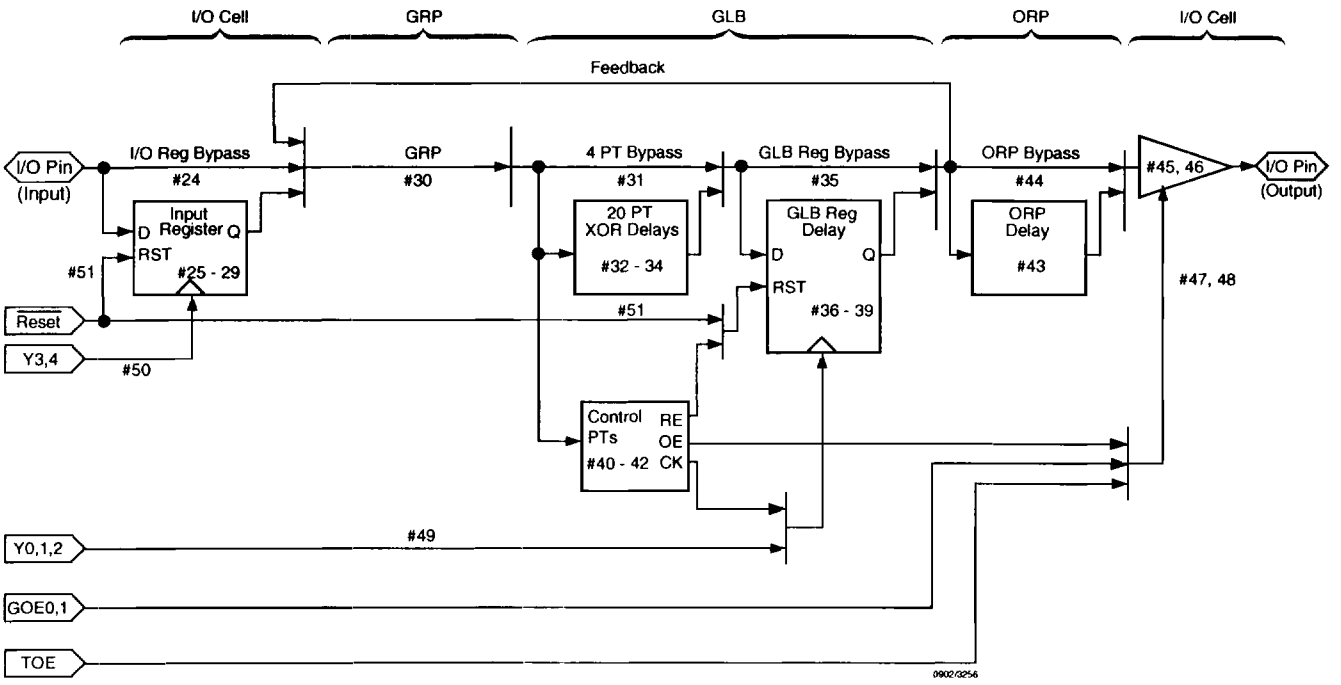
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-70		-50		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	45	Output Buffer Delay	–	2.4	–	3.3	ns
t_{obs}	46	Output Buffer Delay, Slow Slew	–	12.4	–	13.3	ns
t_{oen}	47	I/O Cell OE to Output Enabled	–	7.2	–	9.8	ns
t_{odis}	48	I/O Cell OE to Output Disabled	–	7.2	–	9.8	ns
Clocks							
$t_{gy0/1/2}$	49	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	3.6	3.6	4.9	4.9	ns
$t_{ioy3/4}$	50	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	1.2	5.2	1.6	7.0	ns
Global Reset							
t_{gr}	51	Global Reset to GLB and I/O Registers	–	7.1	–	9.6	ns

Table 2 - 0037A/3256

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI and pLSI 3256 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (tiobp + tgrp + t20ptxor) + (tgsu) - (tiobp + tgrp + tptck(min))
= (#24+ #30+ #33) + (#36) - (#24+ #30+ #42)
8.0 ns = (2.4 + 3.0 + 9.4) + (1.8) - (2.4 + 3.0 + 3.2)

th = Clock (max) + Reg h - Logic
= (tiobp + tgrp + tptck(max)) + (tgh) - (tiobp + tgrp + t20ptxor)
= (#24+ #30+ #42) + (#37) - (#24+ #30+ #33)
2.9 ns = (2.4 + 3.0 + 6.3) + (6.0) - (2.4 + 3.0 + 9.4)

tco = Clock (max) + Reg co + Output
= (tiobp + tgrp + tptck(max)) + (tgco) + (torp + tob)
= (#24 + #30 + #42) + (#38) + (#43 + #45)
2.9 ns = (2.4 + 3.0 + 6.3) + (1.8) + (2.7 + 2.4)

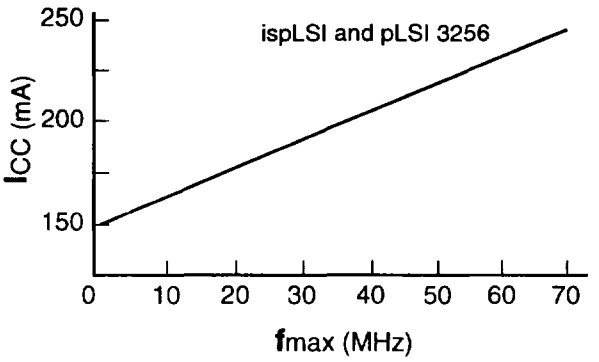
Table 2- 0042-16/3256

Note: Calculations are based on timing specs for the ispLSI 3256-70L.

Power Consumption

Power Consumption in the ispLSI and pLSI 3256 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the pLSI and ispLSI 3256 using the following equation:

I_{CC} = 44 + (# of PTs * 0.18) + (# of nets * Max. freq * 0.013) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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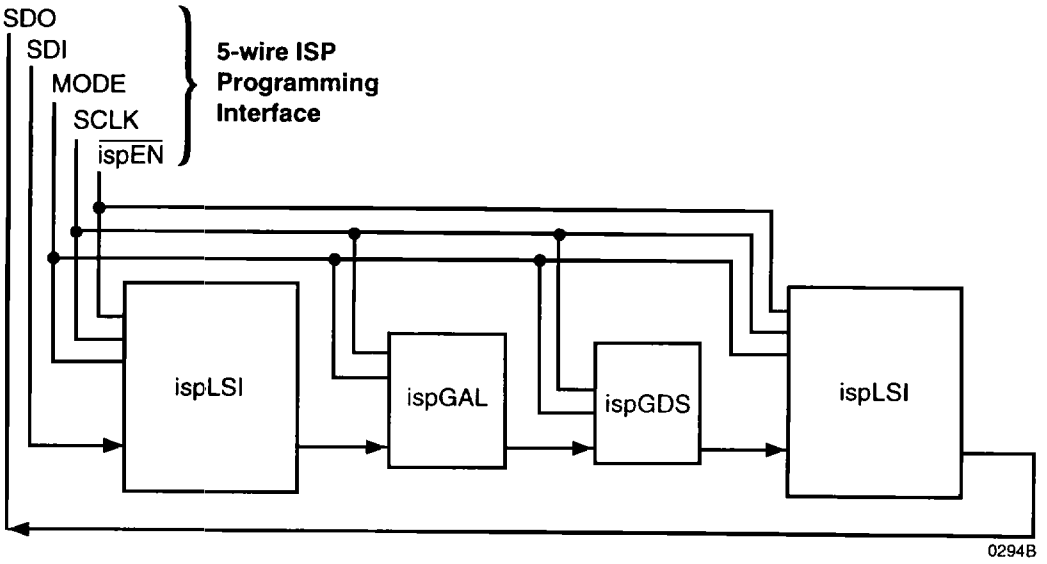
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp Enable (ispEN), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to Lattice's In-System Programmability Manual.

Figure 4. ISP Programming Interface



ISP Programming Voltage/Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCP}	Programming Voltage		4.75	5.0	5.25	V
I_{CCP}	Programming Supply Current		–	50	100	mA
V_{IHP}	Input Voltage High	$\overline{ispEN}$ = Low	2.0	–	V_{CCP}	V
V_{ILP}	Input Voltage Low		0.0	–	0.8	V
I_{IP}	Input Current		–	100	200	µA
V_{OHP}	Output Voltage High	I_{OH} = -3.2 mA	2.4	–	V_{CCP}	V
V_{OLP}	Output Voltage Low	I_{OL} = 5 mA	0.0	–	0.5	V
t_r, t_f	Input Rise and Fall		–	–	0.1	µs
t_{ispen}	$\overline{ispEN}$ to Output 3-State Enabled		–	–	10	µs
t_{ispdis}	$\overline{ispEN}$ to Output 3-State Disabled		–	–	10	µs
t_{su}	Setup Time		0.1	–	–	µs
t_{co}	Clock to Output		–	–	0.1	µs
t_h	Hold Time		0.1	–	–	µs
t_{clkh}, t_{clkl}	Clock Pulse Width, High and Low		0.5	–	–	µs
t_{pwv}	Verify Pulse Width		20	–	–	µs
t_{pwp}	Programming Pulse Width		80	–	160	ms
t_{bew}	Bulk Erase Pulse Width		200	–	–	ms
t_{rst}	Reset Time from Valid V_{CCP}	Rise Time < 50 µs	100	–	–	µs

Table 2 - 0029isp-3256

Figure 5. Timing Waveform for ISP Operation

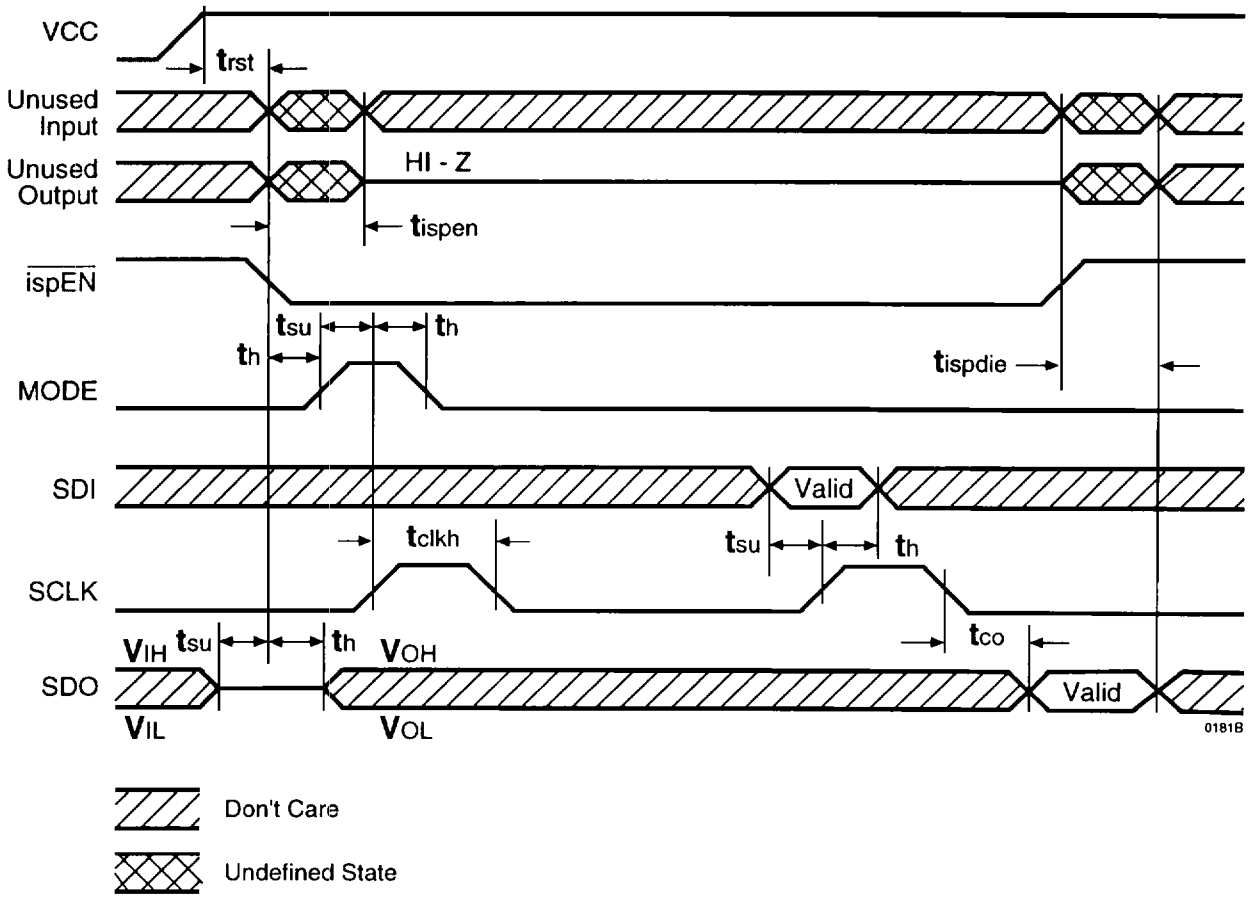


Figure 6. Program, Verify & Bulk Erase Waveform

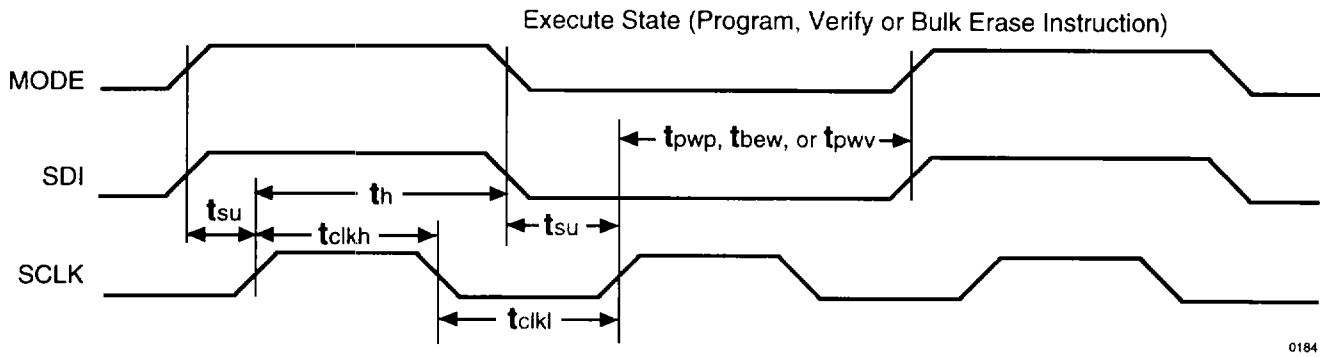
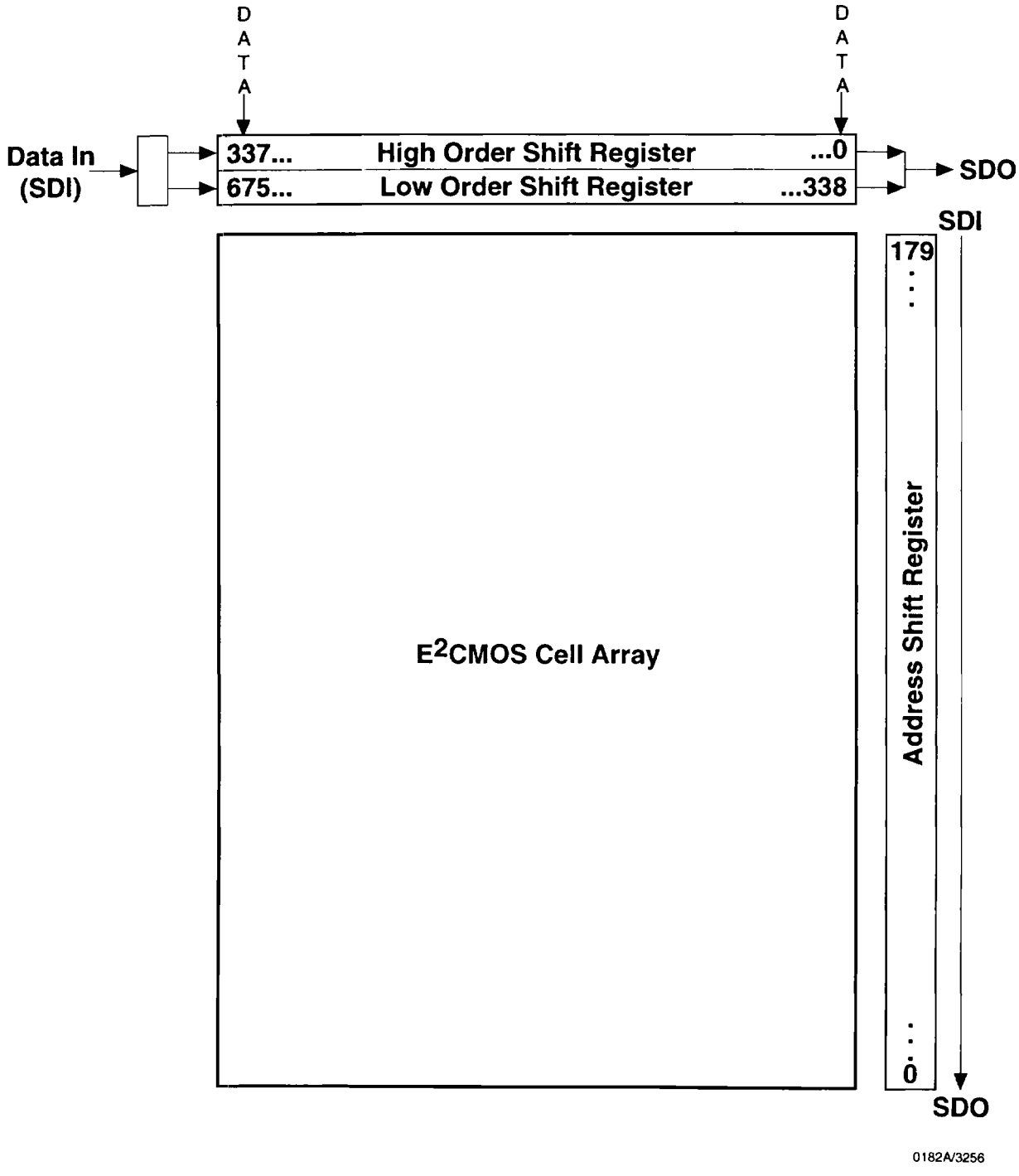


Figure 7. ispLSI 3256 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Boundary Scan

Lattice offers support for the IEEE 1149.1 Boundary Scan specification on the 3000 Family of devices.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{TRST}$) and Test Clock (TCK).

All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells are connected in the following order: TDI to IO63 thru IO32 to Y4, Y3, Y2, Y1, Reset, TOE, GOE1, GOE0, Y0, IO31 thru IO0 to IO64 thru IO127 to TDO.

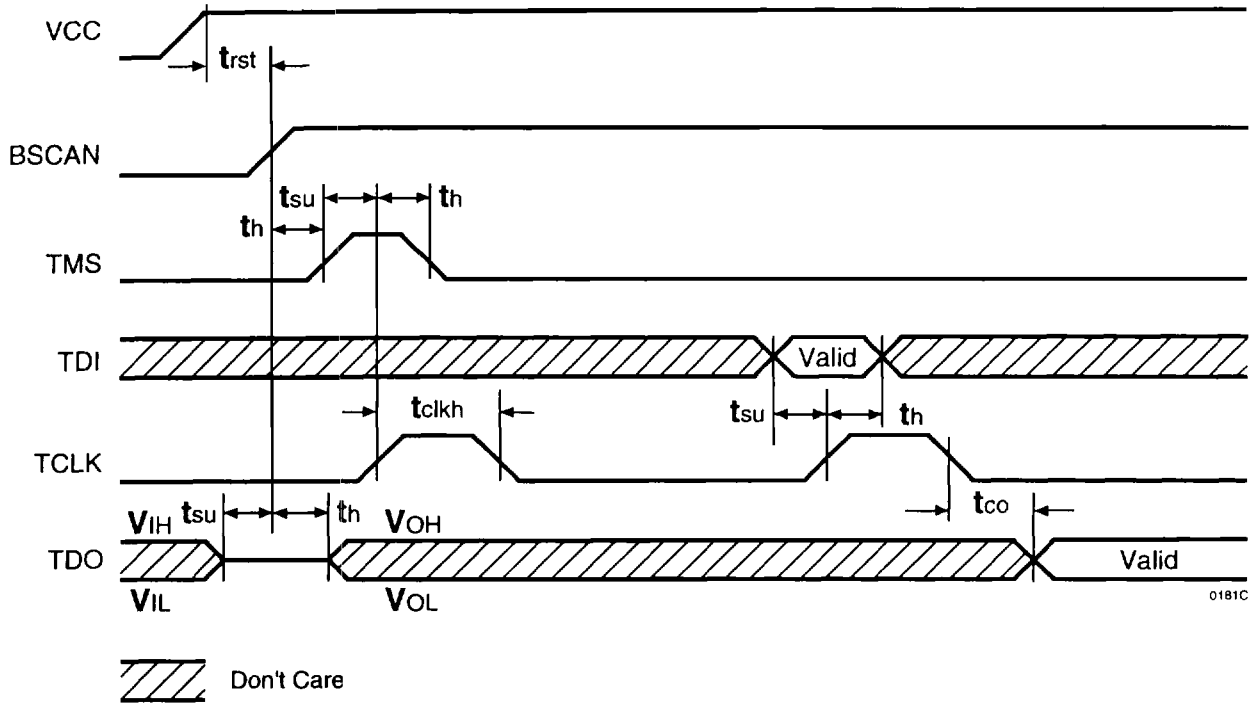
The timing specifications for Boundary Scan are listed below. The waveforms are shown in figure 8.

Boundary Scan Timing Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		60	–	–	ns
t_{co}	Clock to Output		–	–	60	ns

Table 2 - 0028Aisp-3256

Figure 8. Boundary Scan Waveforms



Pin Description

NAME	MQUAD PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	25, 26, 28, 29, 30, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 46, 47, 48, 49, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 70, 72, 73, 74, 75, 76, 77, 78, 79, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 105, 106, 108, 109, 110, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 126, 127, 128, 129, 130, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 144, 145, 146, 147, 148, 149, 150, 152, 153, 154, 155, 156, 157, 158, 159, 160, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15, 16, 17	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	100 and 99 98	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	20 18, 19, 103 102, 101	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$** TDI/SDI* TCLK/SCLK* TMS/MODE* $\overline{\text{TRST}}$ TDO/SDO*	21 22 23 24 97 104	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. Input - Test Reset, active low to reset the Boundary Scan State Machine. Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND VCC	1, 10, 27, 45, 63, 81, 107, 125, 143 12, 31, 51, 71, 91, 111, 131, 151	Ground (GND) V_{CC}

Table 2 - 0002Bisp/3256

* ispLSI 3256 only

** $\overline{\text{ispEN}}$ for ispLSI 3256 only, NC for pLSI 3256 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Description

NAME	CPGA PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 4 I/O 5 - I/O 9 I/O 10 - I/O 14 I/O 15 - I/O 19 I/O 20 - I/O 24 I/O 25 - I/O 29 I/O 30 - I/O 34 I/O 35 - I/O 39 I/O 40 - I/O 44 I/O 45 - I/O 49 I/O 50 - I/O 54 I/O 55 - I/O 59 I/O 60 - I/O 64 I/O 65 - I/O 69 I/O 70 - I/O 74 I/O 75 - I/O 79 I/O 80 - I/O 84 I/O 85 - I/O 89 I/O 90 - I/O 94 I/O 95 - I/O 99 I/O 100 - I/O 104 I/O 105 - I/O 109 I/O 110 - I/O 114 I/O 115 - I/O 119 I/O 120 - I/O 124 I/O 125 - I/O 127	G1, G2, G3, E1, F2, F3, C1, E2, E3, D2, D3, B2, C3, C4, B3, B1, B4, C5, A3, B5, C6, A4, B6, A5, C7, A6, A7, C8, B8, B9, C9, A9, A10, B10, A11, B11, A12, C11, A13, B12, A14, A15, A16, C13, B14, B15, C14, B16, C15, D15, A17, D16, E15, B17, C17, E16, F15, D17, E17, F17, G16, G17, H15, H16, L16, M17, N17, M16, P17, R17, N16, S17, N15, P16, P15, S16, R15, R14, S15, T17, S14, R13, T15, S13, R12, T14, S12, T13, R11, T12, T11, R10, S10, S9, R9, T9, T8, S8, T7, S7, T6, R7, T5, S6, T4, T3, T2, R5, S4, S3, R4, S2, R3, P3, T1, P2, N3, S1, R1, N2, M3, P1, N1, M1, L2, L1, K3, K2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1	J17 and J15	Global Output Enable input pins.
TOE	J16	Test output enable pin.
$\overline{\text{RESET}}$	J3	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0, Y1 and Y2	K1, J2, K15	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device.
Y3 and Y4	K16, K17	Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$**	J1	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
TDI/SDI*	H1	Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine.
TCLK/SCLK*	H2	Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
TMS/MODE*	H3	Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine.
$\overline{\text{TRST}}$	H17	Input - Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO*	L17	Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND	F1, C2, A2, B7, C10, B13, C16, F16, L15, R16, T16, S11, S5, R8, R2, M2	Ground (GND)
VCC	D1, A8, G15, C12, M15, T10, L3, R6	V_{CC}

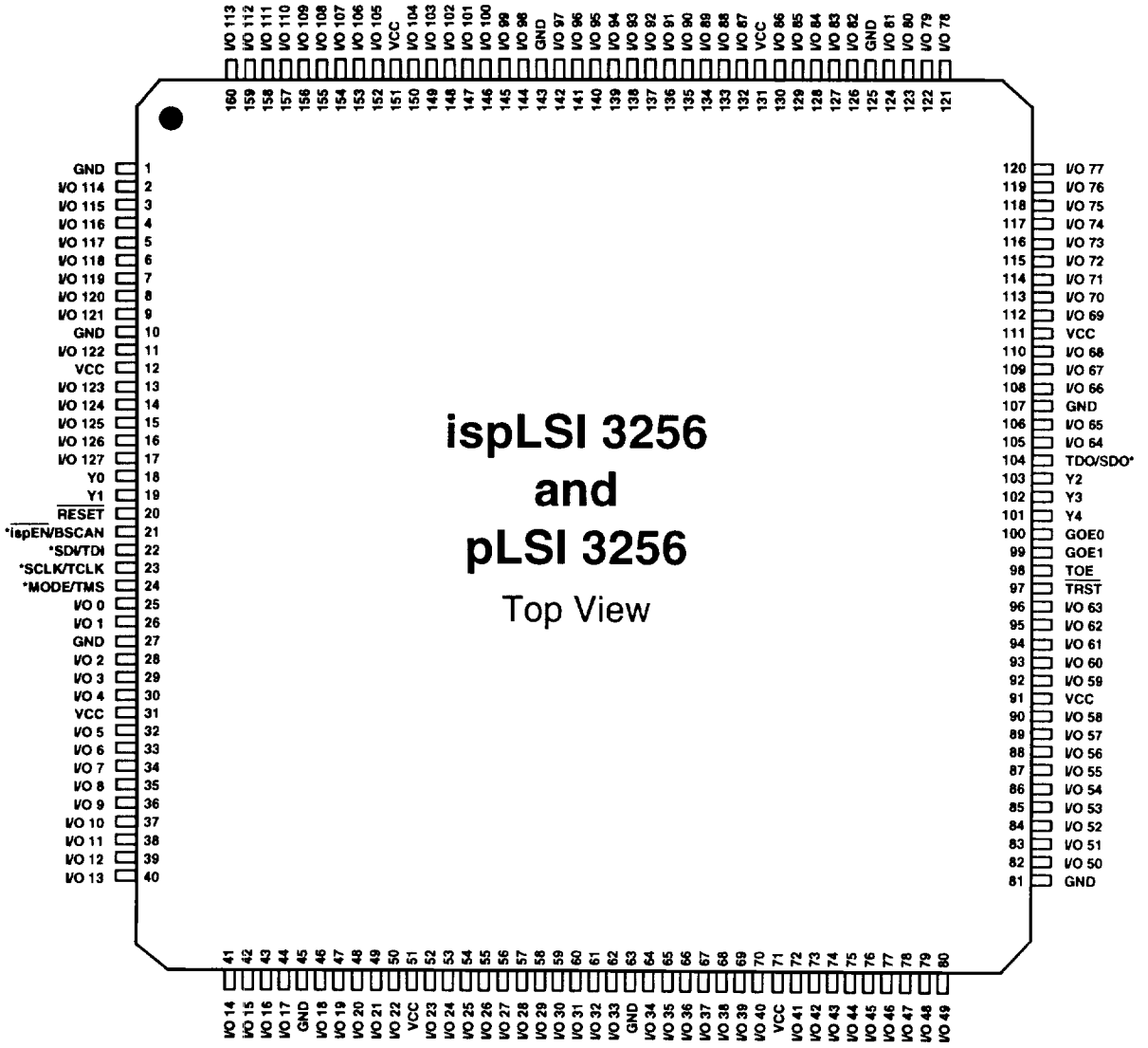
Table 2 - 0002isp/3256

* ispLSI 3256 only

** $\overline{\text{ispEN}}$ for ispLSI 3256 only, NC for pLSI 3256 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

Pin Configuration

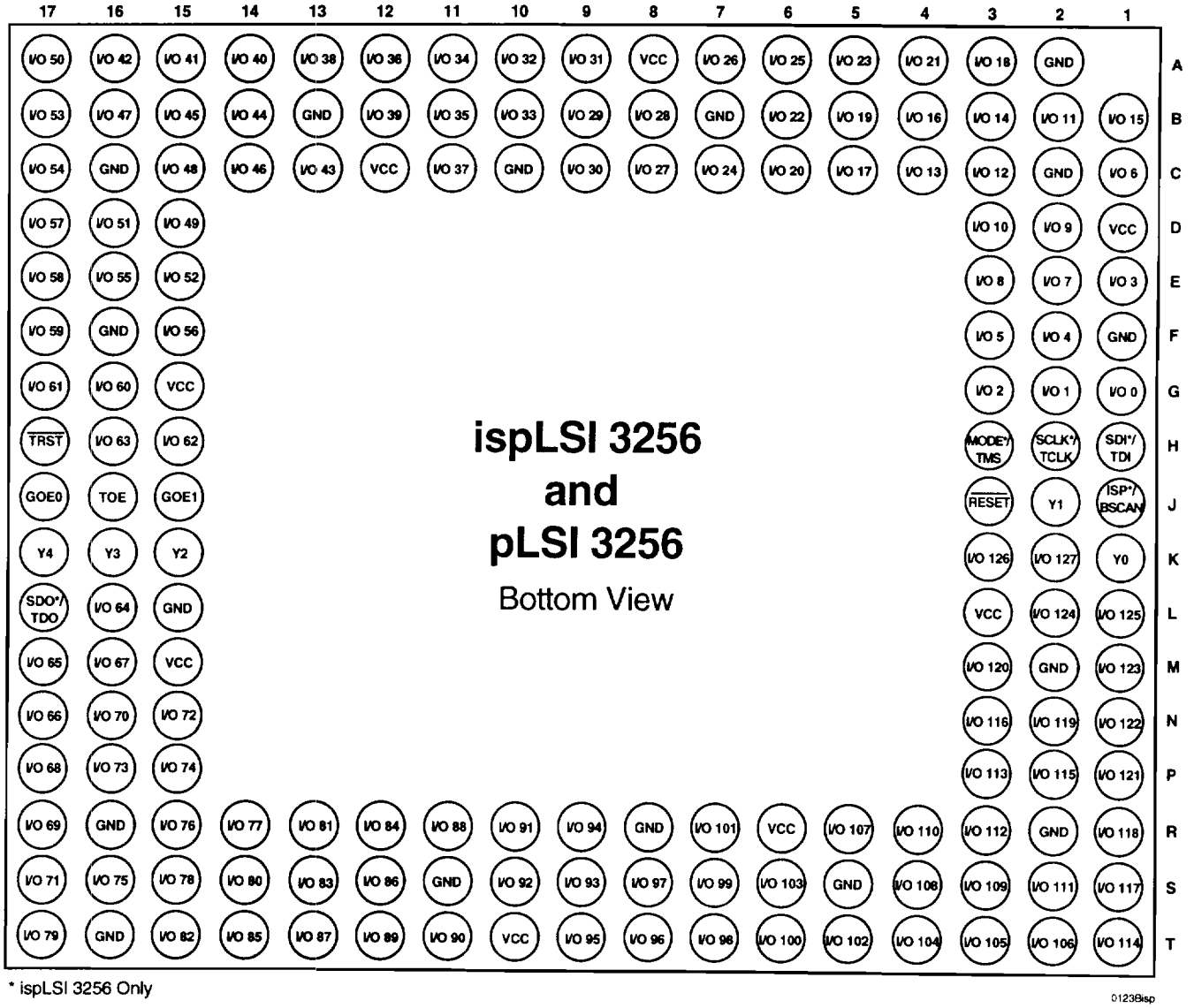
ispLSI and pLSI 3256 160-pin MQUAD Pinout Diagram



*ispLSI 3256 Only

Pin Configuration

ispLSI and pLSI 3256 167-Pin CPGA Pinout Diagram



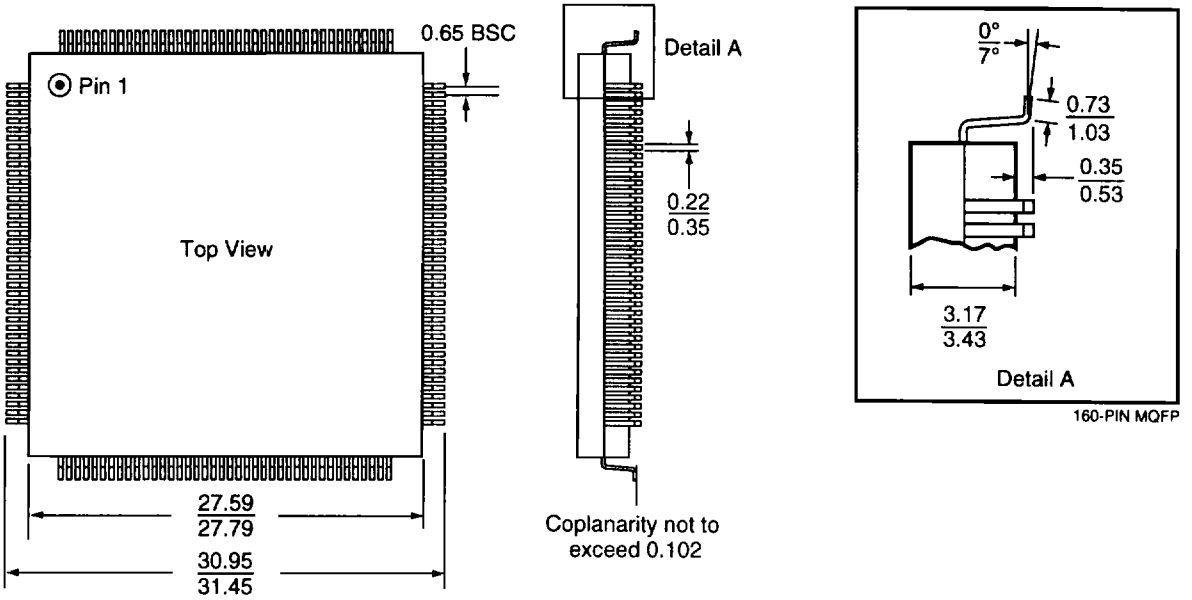
* ispLSI 3256 Only

0123Bisp

Package Diagram

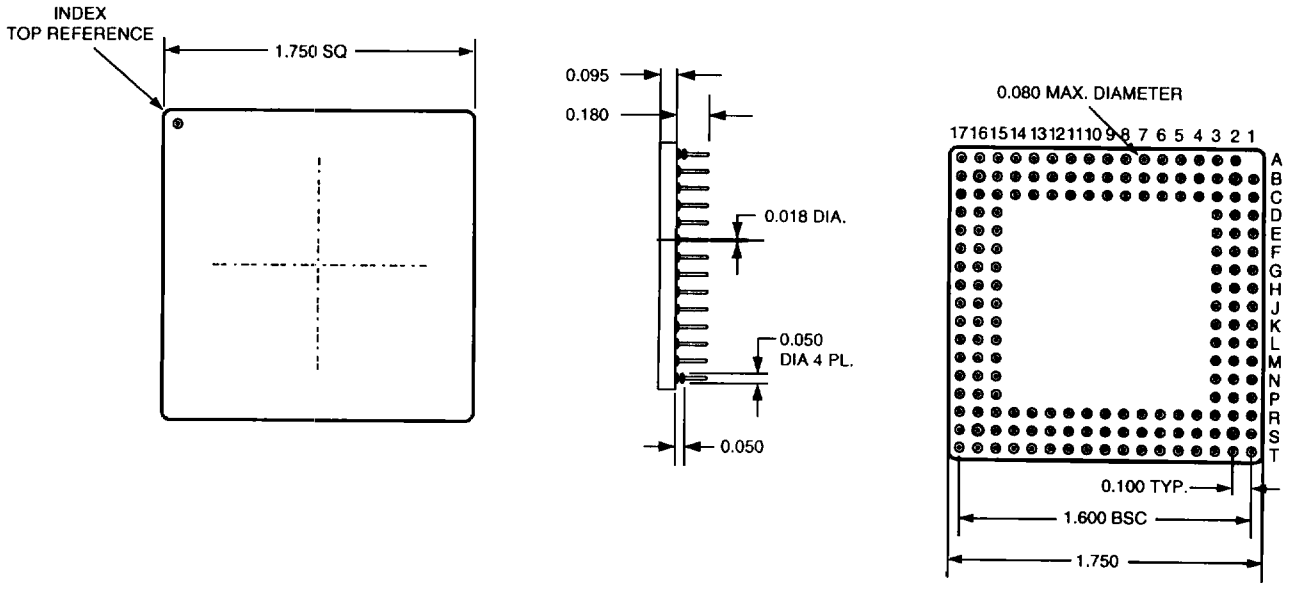
160-Pin MQUAD Package

Dimensions in Millimeters Min./Max.

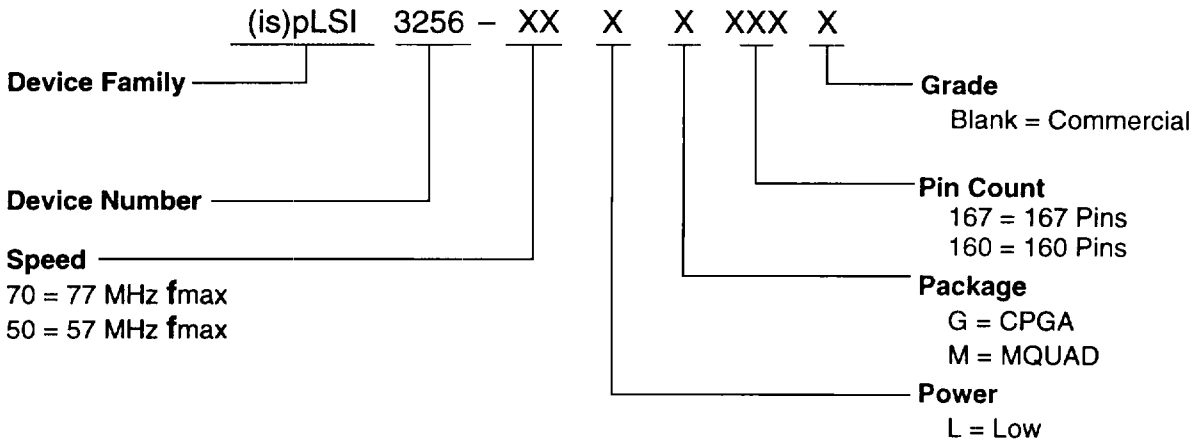


167-Pin CPGA Package

Dimensions in Inches



Part Number Description



0212Aisp/3256

Ordering Information

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	77	15	ispLSI 3256-70LM160	160-Pin MQUAD
	77	15	ispLSI 3256-70LG167	167-Pin CPGA
	57	20	ispLSI 3256-50LM160	160-Pin MQUAD
	57	20	ispLSI 3256-50LG167	167-Pin CPGA
pLSI	77	15	pLSI 3256-70LM160	160-Pin MQUAD
	77	15	pLSI 3256-70LG167	167-Pin CPGA
	57	20	pLSI 3256-50LM160	160-Pin MQUAD
	57	20	pLSI 3256-50LG167	167-Pin CPGA

Table 2 - 0041A-08isp/3256